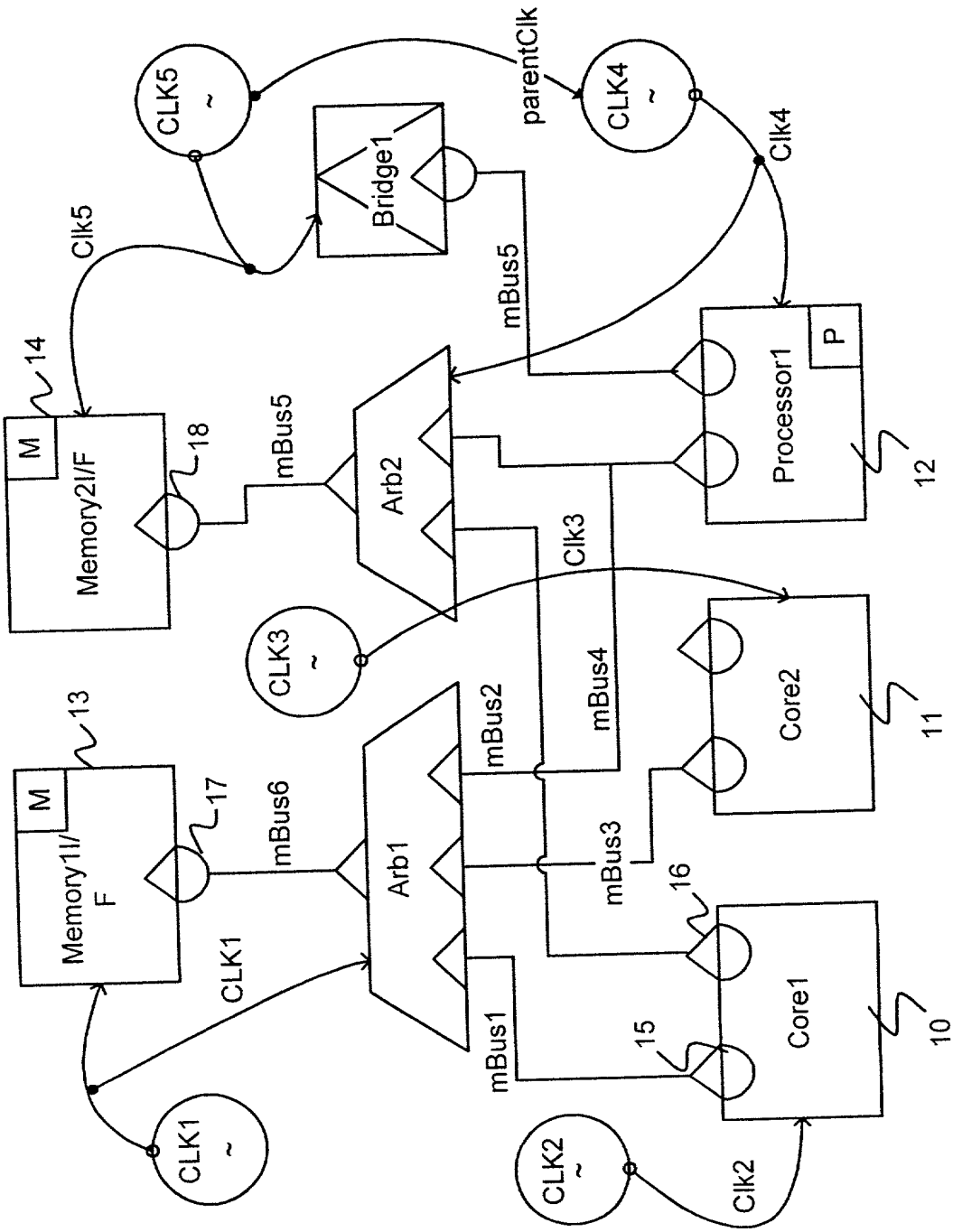
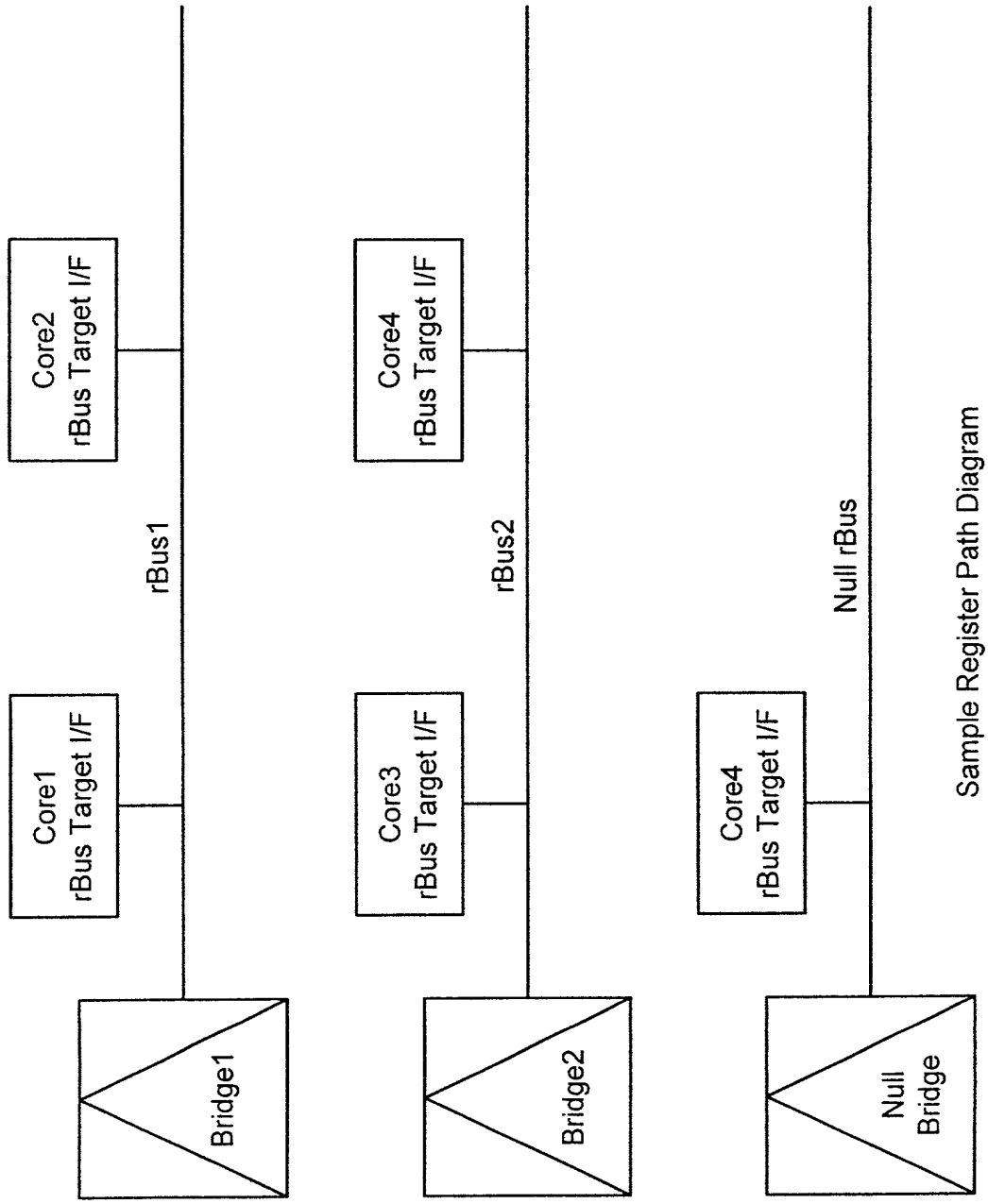

CLK5
parentClk
CLK4
Bridge1
Clk5
Clk4
mBus5
14
M
Memory2I/F
18
mBus5
Arb2
Processor1
P
12
CLK3
Clk3
13
M
Memory1I/F
17
mBus6
Arb1
mBus2
mBus4
Core2
11
mBus3
16
CLK1
mBus1
15
Core1
10
CLK2
Clk2

FIG. 1



Sample Register Path Diagram

FIG. 2

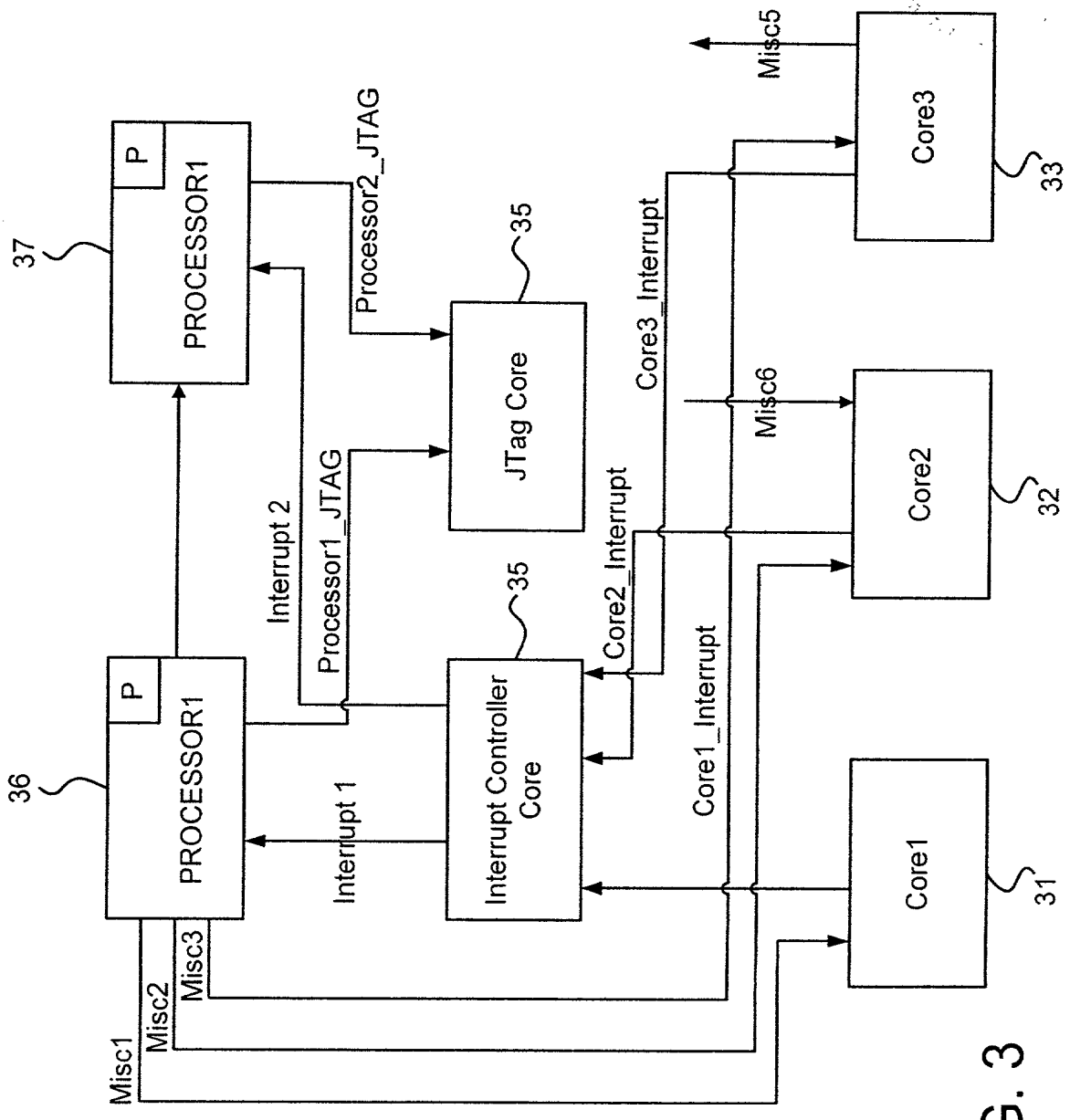

P
PROCESSOR1
37
Processor2_JTAG
35
JTag Core
Misc5
Core3
33
Core3_Interrupt
Misc6
Core2
32
Core2_Interrupt
Core1_Interrupt
Interrupt 2
Processor1_JTAG
35
Interrupt Controller Core
Interrupt 1
Core1
31
36
P
PROCESSOR1
Misc3
Misc2
Misc1

FIG. 3

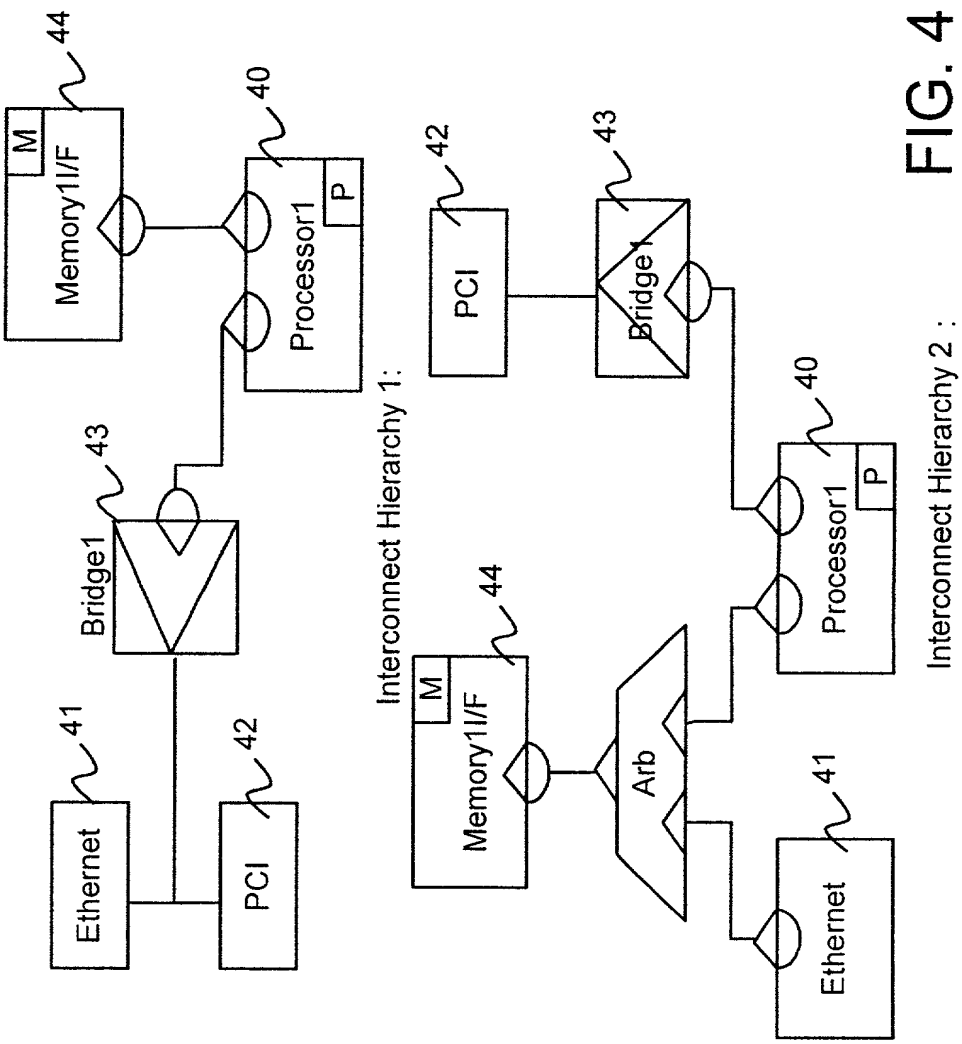

Interconnect Hierarchy 1:
Memory1I/F
M
44
Processor1
P
40
Bridge1
43
Ethernet
41
PCI
42
Interconnect Hierarchy 2 :
PCI
42
Bridge1
43
Memory1I/F
M
44
Arb
Processor1
P
40
Ethernet
41

FIG. 4

State	CLK2	CLK5	CLK6	Strobe5	ClrStrobe5	Sample5	Strobe6	ClrStrobe 6	Sample 6
0	0	0	0	0	1	1	0	0	1
1	1	1	1	0	1	1	0	0	1
2	0	0	1	1	0	0	0	1	0
3	1	0	1	1	0	0	0	1	0
4	0	0	0	0	0	1	1	0	0
5	1	1	0	0	0	1	1	0	0
6	0	1	0	0	1	0	0	0	1
7	1	1	1	0	1	0	0	0	1
8	0	0	1	1	0	0	0	1	0
9	1	0	1	1	0	0	0	1	0
10	0	0	0	0	1	1	1	0	0
11	1	1	0	0	1	1	1	0	0
12	0	0	0	1	0	0	0	0	1
13	1	0	1	1	0	0	0	0	1
14	0	0	1	0	0	1	0	1	0
15	1	1	1	0	0	1	0	1	0
16	0	1	0	0	1	0	1	0	0
17	1	1	0	0	1	0	1	0	0
18	0	0	0	1	0	0	0	0	1
19	1	0	1	1	0	0	0	0	1
20	0	0	1	0	1	1	0	1	0
21	1	1	1	0	1	1	0	1	0
22	0	0	0	1	0	0	1	0	0
23	1	0	0	1	0	0	1	0	0
24	0	0	0	0	0	1	0	0	1
25	1	1	1	0	0	1	0	0	1
26	0	1	1	0	1	0	0	1	0
27	1	1	1	0	1	0	0	1	0
28	0	0	0	1	0	0	1	0	0
29	1	0	0	1	0	0	1	0	0

FIG. 5

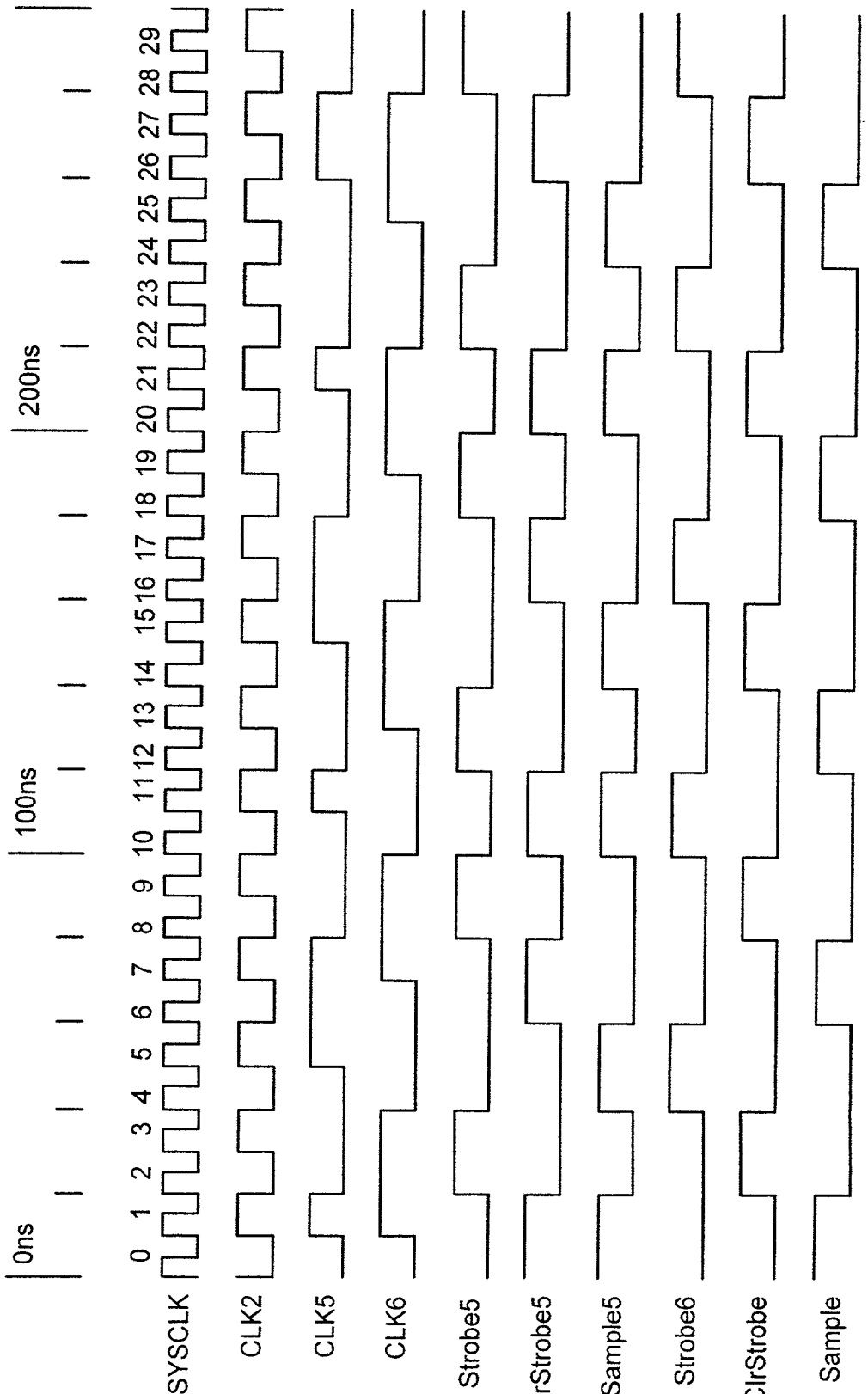

0ns
100ns
200ns
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
SYSCLK
CLK2
CLK5
CLK6
Strobe5
ClrStrobe5
Sample5
Strobe6
ClrStrobe
Sample

FIG. 6

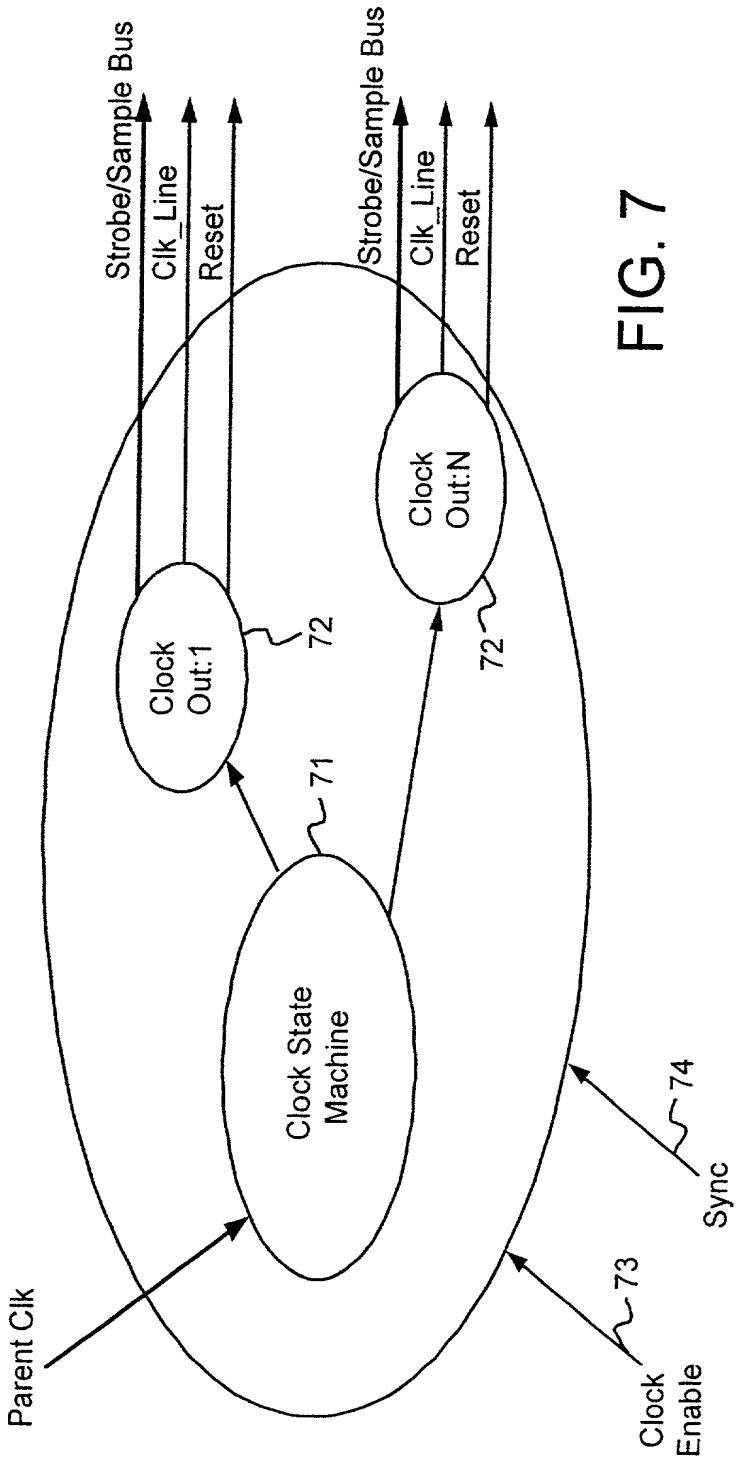

Strobe/Sample Bus
Clk_Line
Reset
Strobe/Sample Bus
Clk_Line
Reset
Clock Out:1
72
Clock Out:N
72
71
Clock State Machine
Parent Clk
73
Clock Enable
74
Sync

FIG. 7

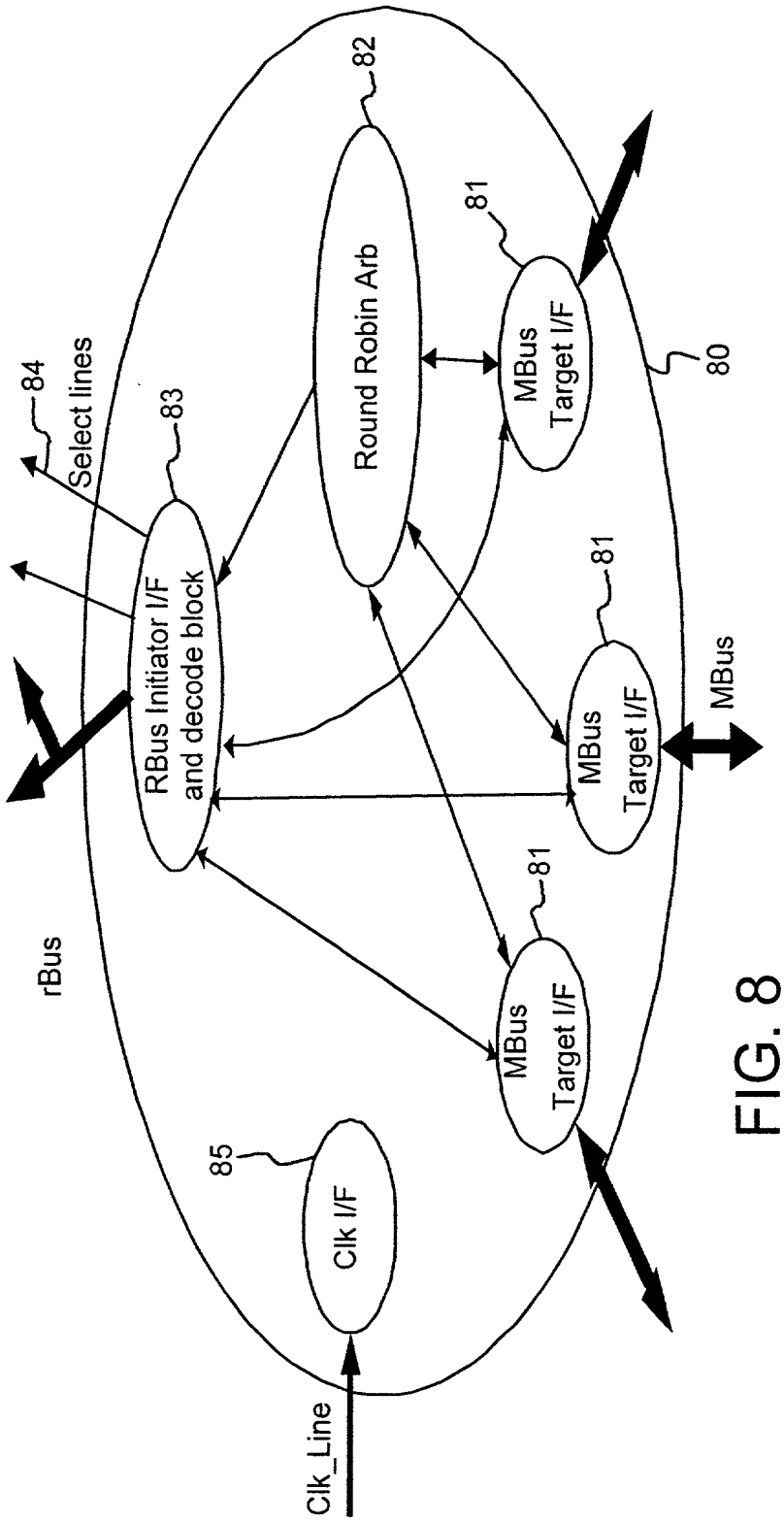

rBus
RBus Initiator I/F and decode block
83
84
Select lines
Round Robin Arb
82
MBus Target I/F
81
MBus Target I/F
81
MBus Target I/F
81
MBus
80
Clk I/F
85
Clk_Line

FIG. 8

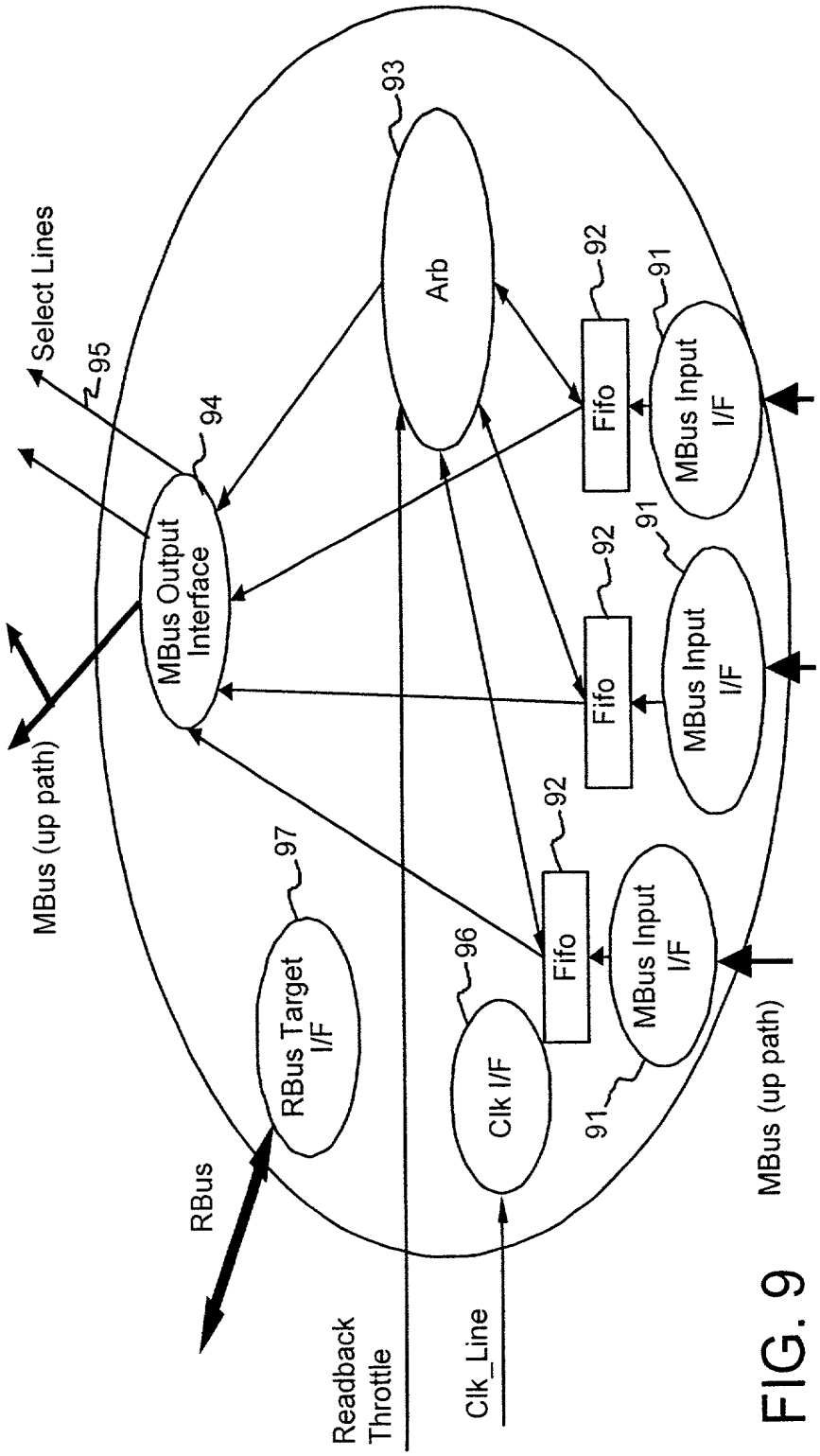

Select Lines
95
94
MBus Output Interface
MBus (up path)
93
Arb
92
Fifo
91
MBus Input I/F
92
Fifo
91
MBus Input I/F
92
Fifo
91
MBus Input I/F
97
RBus Target I/F
96
Clk I/F
RBus
Readback Throttle
Clk_Line
MBus (up path)

FIG. 9

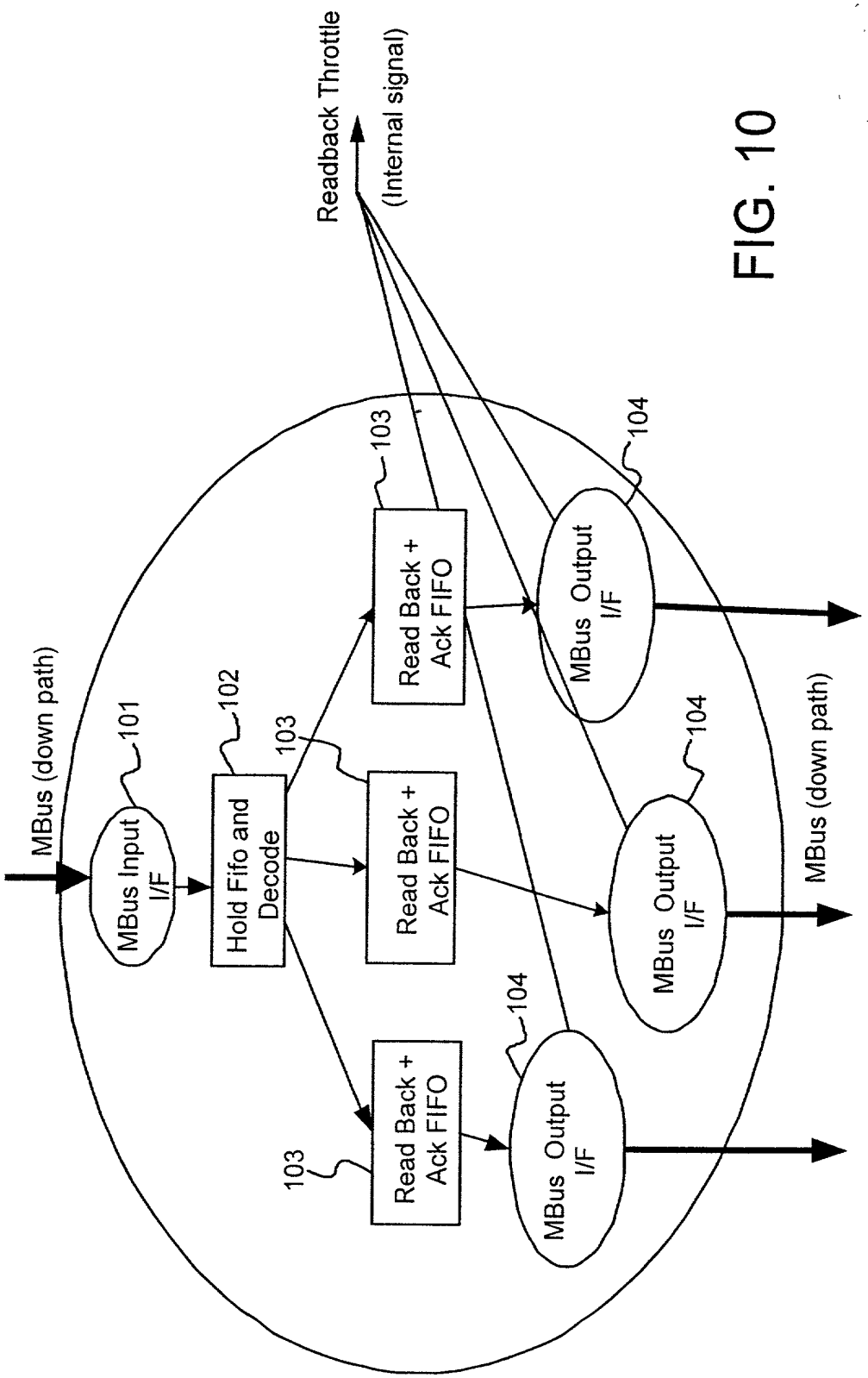

MBus (down path)
MBus Input I/F
101
Hold Fifo and Decode
102
103
Read Back + Ack FIFO
Read Back + Ack FIFO
Read Back + Ack FIFO
103
103
MBus Output I/F
MBus Output I/F
MBus Output I/F
104
104
104
Readback Throttle
(Internal signal)
MBus (down path)

FIG. 10

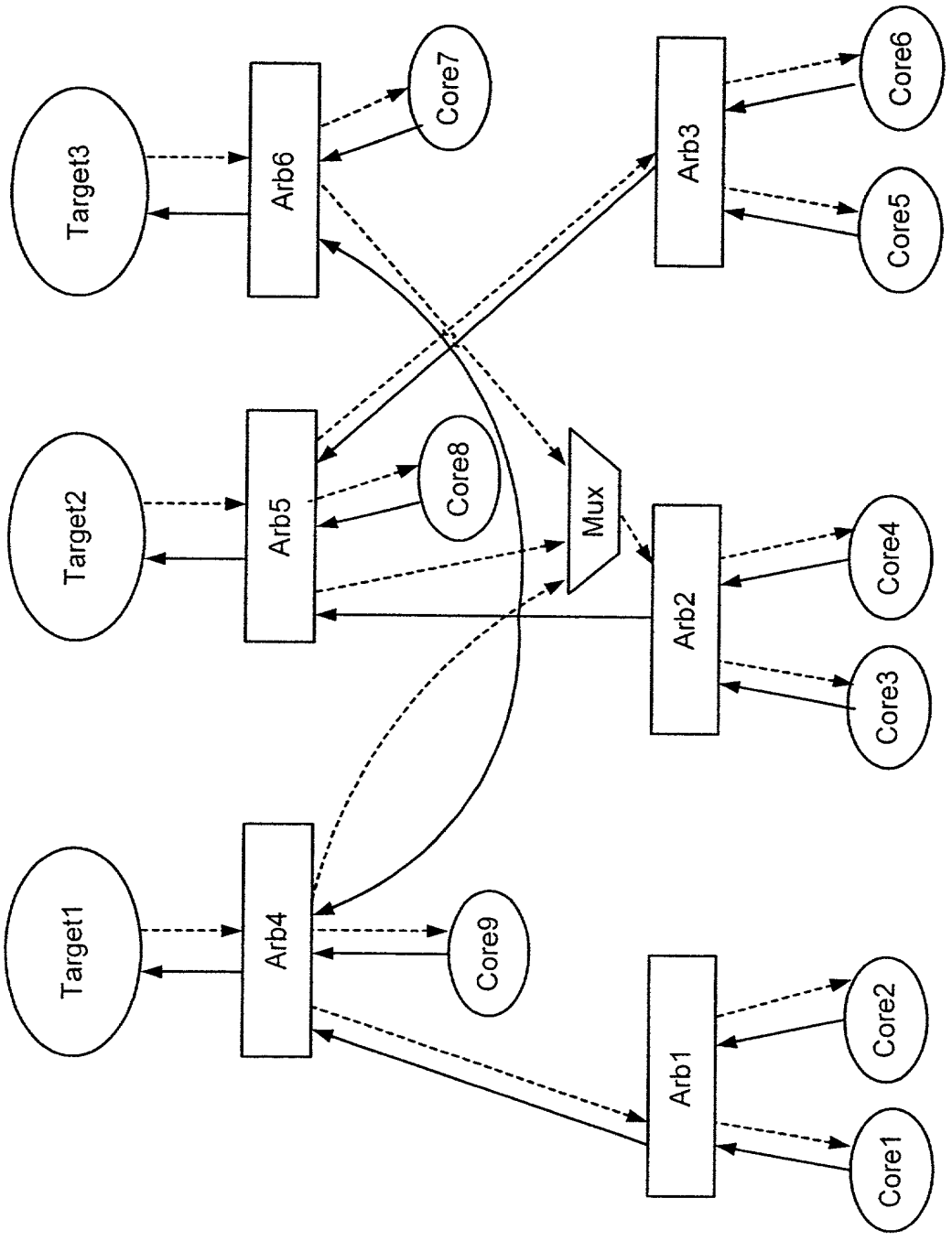

Target1
Target2
Target3
Arb4
Arb5
Arb6
Arb1
Arb2
Arb3
Mux
Core1
Core2
Core3
Core4
Core5
Core6
Core7
Core8
Core9

FIG. 11

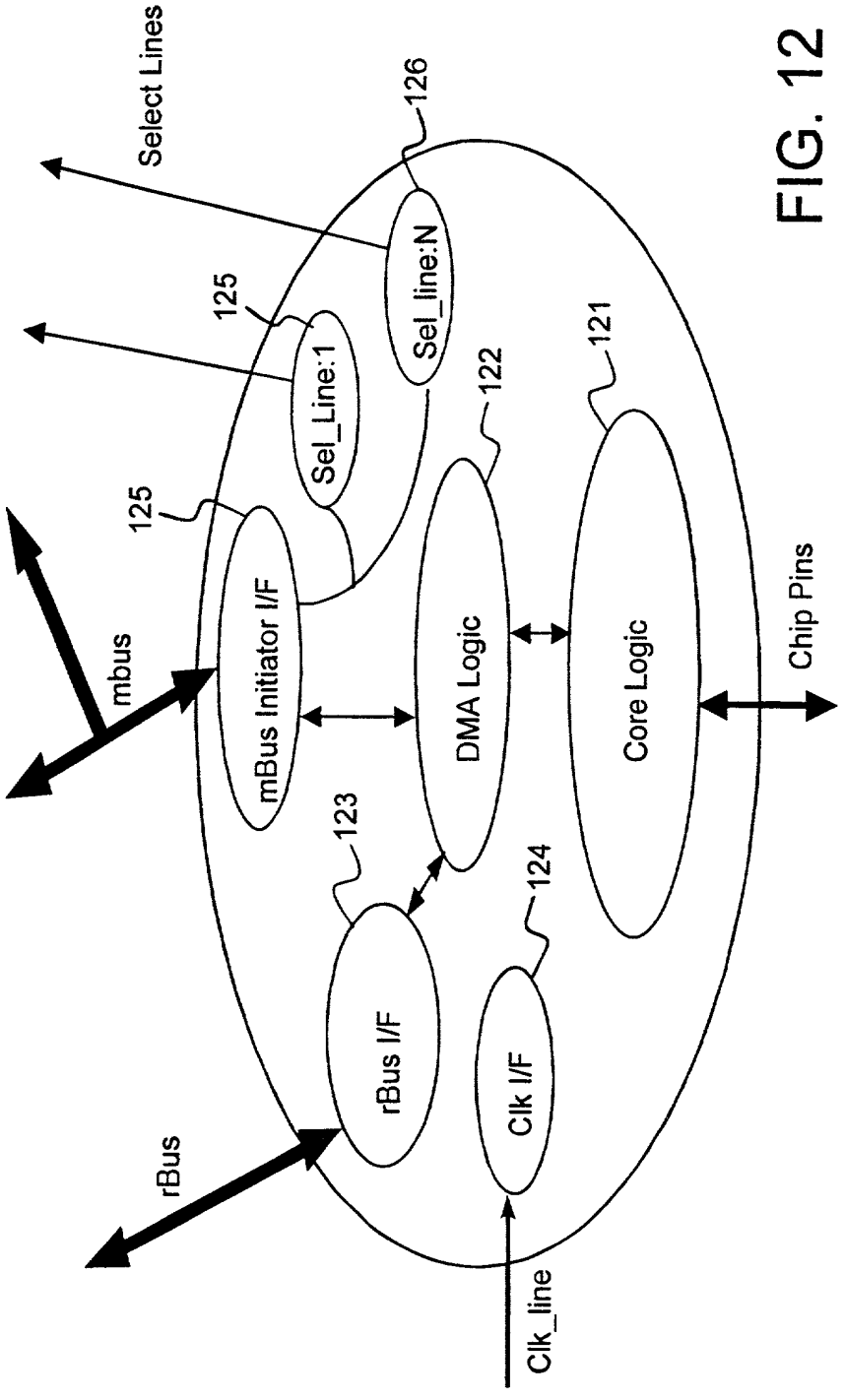

Select Lines
126
Sel_line:N
125
Sel_Line:1
125
mBus Initiator I/F
122
DMA Logic
121
Core Logic
Chip Pins
mbus
123
rBus I/F
124
Clk I/F
rBus
Clk_line

FIG. 12

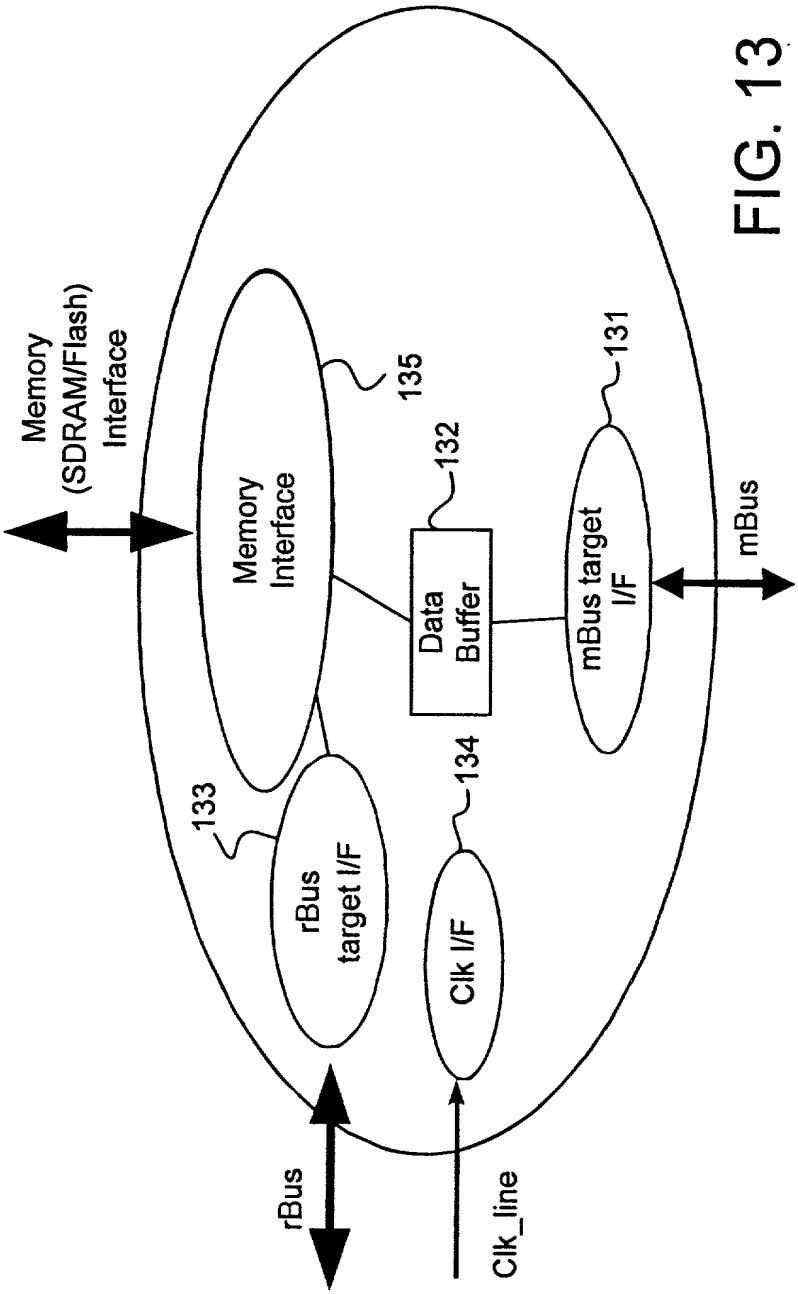

Memory
(SDRAM/Flash)
Interface
Memory
Interface
135
132
Data
Buffer
131
mBus target
I/F
mBus
133
rBus
target I/F
134
Clk I/F
rBus
Clk_line

FIG. 13